ABSTRACT

0031 A method for forming a dual damascene opening to protect a low-K dielectric insulating layer including providing a semiconductor process wafer comprising a via opening extending though a thickness portion of at least one dielectric insulating layer; depositing a first dielectric layer stack layer comprising at least one dielectric insulating layer over the at least one dielectric insulating to seal the via opening; blanket depositing a second dielectric layer stack comprising at least one dielectric layer to form a hardmask over and contacting the first dielectric layer stack; photolithographically patterning and etching through a thickness of the hardmask and the first dielectric layer stack to form a trench opening etching pattern overlying and encompassing the via opening while leaving the via opening sealed; and, etching through a thickness portion of the at least one dielectric insulating layer to form a dual damascene opening.